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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,990	12/03/2003	Mario Di Ronza	LLP103US	5035

29393 7590 09/22/2006

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 09/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,990	RONZA ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 15-28* is/are rejected.

7)☒ Claim(s) *9-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/3/03* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/5/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 4/5/04 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Drawings

The drawings are objected to because descriptive labels other than numerical are needed for figures 1-2. See 37 CFR 1.84(o). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top

margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

This abstract is too long.

Allowable Subject Matter

Claims 9-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 7, 8, 15, 16, 19, 20, 22, and 24-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Augarten U.S. Patent No. 5,588,115.

As per claim 1, Augarten teaches the claimed method for testing an integrated memory having a main data memory with a plurality of data memory units, comprising: a) addressing a data memory unit by applying an address of the data memory unit to an address bus operably coupled to the main data memory; b) applying input test data to a data bus operably coupled to the main data memory to test the addressed data memory unit; c) reading out output test data from the addressed data memory unit; d) comparing the output test data with expected desired output test data; e) storing the applied address, the expected desired output test data, and the output test data as information in a redundancy analysis memory if a deviation of the output test data from the desired output test data occurs; f) providing first redundant areas in the redundancy analysis

memory and providing at least second redundant areas outside the redundancy analysis memory; and g) determining a repair strategy by means of the first and second redundant areas on the basis of the information stored in the redundancy analysis memory. (Column 2 lines 55 through column 3 line 10)

As per claim 2, Augarten teaches dividing the main data memory, for testing purposes, into sub-areas that are tested separately. (Column 3 lines 31-41)

As per claim 3, Augarten teaches dividing the main data memory into sub-areas of identical size or of different size, and determining a repair strategy for each sub-area, the testing of the entire main data memory being carried out in an iterative manner by the sub-areas being tested one after the other. (Column 3 lines 56-66)

As per claim 4, Augarten teaches the first redundant areas of the redundancy analysis memory is provided for repairing each sub-area and the at least second redundant areas are provided for only one sub-area in each case. (Column 6 lines 15-26)

As per claim 7, Augarten teaches employing the first redundant areas, depending on the number of detected deviations of the output test data from the expected desired output test data before the at least second redundant areas of the integrated memory for the determination of the repair strategy. (Column 6 lines 15-26)

As per claim 8, Augarten teaches exclusively employing first redundant areas of the redundancy analysis memory for the repair strategy if a test run is ended and a storage capacity of the redundancy analysis memory is occupied at most maximally with information items of the defective data memory units detected. (Column 5 lines 11-20)

As per claim 15, Augarten teaches the information items as to which first redundant areas and/or which second redundant areas and/or are utilized for an intermediate repair strategy or a concluding repair strategy, and the information therein are written to memory registers operably coupled to the computing unit. (Column 6 lines 15-26)

As per claim 16, Augarten teaches executing a plurality of test runs with identical or different test algorithms or, after an interruption of a single test run, a test algorithm for testing is chosen that is identical to or different from the test algorithm with which the testing is carried out before the interruption of the single test run. (Column 5 lines 57-66)

As per claim 19, Augarten teaches during the reading out of the information items stored in the redundancy analysis memory, the clock frequency with which the integrated memory is tested is reduced. (Column 4 lines 5-26)

As per claim 20, Augarten teaches a data width of a first redundant area comprises an interval which extends from a single bit up to a number of bits forming an entire word; and wherein a data width of a second redundant area comprises an interval that extends from a single bit up to a number of bits forming an entire row or a plurality of rows, or an entire column or a plurality of entire columns. (Column 6 lines 15-30)

As per claim 22, Augarten teaches identifying defects in the second redundant areas that are used for an intermediate repair strategy, and replacing the second redundant areas with other second redundant areas and/or first redundant areas. (Column 6 lines 15-30)

As per claim 24, Augarten teaches an integrated memory, comprising: a plurality of data memory units arranged in a memory cell array; a plurality of row lines and column lines, the plurality of row lines having regular and redundant row lines and the plurality of column lines having regular and redundant column lines, respectively; a self-test unit operable, in the event of an access to a row line, to check the contents of a selected data memory unit for the correctness of data therein and operable to store information items associated therewith; a redundancy analysis memory comprising first redundant areas, the redundancy analysis memory operably coupled to the self-test unit and the information items of non-correct data memory units being stored therein; second redundant areas arranged outside the redundancy analysis memory; and a computing unit operably coupled to the self-test unit and the redundancy analysis memory, the computing unit operable to determine a repair strategy based on the information items stored in the redundancy analysis memory. (Column 2 line 55- column 3 line 10)

As per claim 25, Augarten teaches an algorithm unit operably coupled to the self-test unit and the computing unit and operable to select test algorithms. (Column 1 lines 20-25)

As per claim 26, Augarten teaches a data width of a first redundant area comprises an interval that extends from a single bit up to a number of bits forming an entire word; and wherein a data width of a second redundant area comprises an interval that extends from a single bit up to a number of bits forming an entire row or a plurality of rows, or an entire column or a plurality of columns. (Column 6 lines 15-30)

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 5, 6, 17, 18, 21, 23, 27, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Augarten U.S. Patent No. 5,588,115.

As per claims 5, 6, 27 and 28, Augarten teaches the memory is divided into sub areas (regions, column 3 lines 5-10) therefore it would have been obvious to a person having ordinary skill in the art to have used one of the divided regions to replace bad areas of

the other memories either bit by bit or row and column.

As per claim 17, Augarten teaches using test algorithms are used for identifying defects (column 1 lines 20-25) however a person having ordinary skill in the art would be aware that it requires different patterns to identify different types of faults in a memory.

As per claim 18, it is well known in the art for memories to be tested at the operational frequency of the chip in order to identify any delay faults that would not be identified at a slower clock speed.

As per claim 21, Augarten teaches executing the repair strategy and after the repair of the integrated memory, writing the information items of the activated first redundant areas and/or the second redundant areas (column 6 lines 15-30) however does not disclose writing the defects to a nonvolatile memory. It is however common in the art to store information such as this in a nonvolatile memory in order that it not be lost when the chip is powered down.

As per claim 23, it is well known in the art to use repair methods as taught by Augarten (column 6 lines 15-20) such as remapping faulty memory elements with test methods that use error-detecting and error-correcting codes.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent No. 6,469,932 Roohparvar et al.

This patent teaches a flash memory device incorporating redundant rows. The memory device includes a memory array, control circuitry and a register. The control circuitry controls operations to the memory array. The register stores an address of a defect in the memory array and data indicating a type of defect associated with the address.

U.S. Patent No. 6,731,550 McClure

This patent teaches defective memory cells are individually replaced. Instead of providing entire rows and/or columns of redundant memory cells, only a limited number of redundant storage elements are needed in the memory device in order to suitably replace isolated memory cells that are defective.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt
Primary Examiner
Art Unit 2138